



STD3NK80Z, STD3NK80Z-1 STF3NK80Z, STP3NK80Z

N-channel 800 V, 3.8 Ω , 2.5 A, TO-220, TO-220FP, DPAK, IPAK
Zener-protected SuperMESH™ Power MOSFET

Features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STP3NK80Z	800 V	< 4.5 Ω	2.5 A
STF3NK80Z	800 V	< 4.5 Ω	2.5 A
STD3NK80Z	800 V	< 4.5 Ω	2.5 A
STD3NK80Z-1	800 V	< 4.5 Ω	2.5 A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

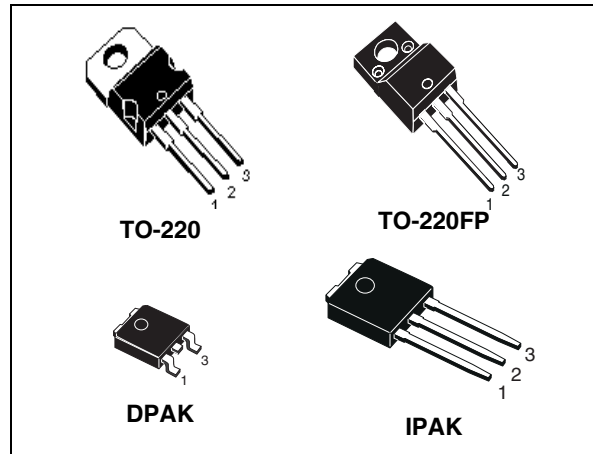


Figure 1. Internal schematic diagram

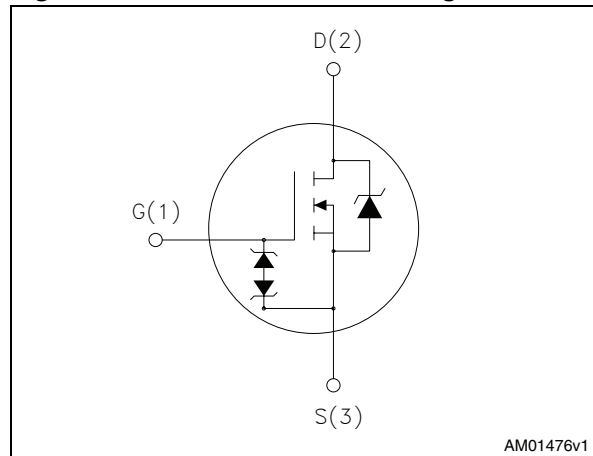


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP3NK80Z	P3NK80Z	TO-220	Tube
STF3NK80Z	F3NK80Z	TO-220FP	Tube
STD3NK80ZT4	D3NK80Z	DPAK	Tape and reel
STD3NK80Z-1	D3NK80Z	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK IPAK	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	800		V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	800		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.5	2.5 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.57	1.57 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	10	10 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	25	W
	Derating factor	0.56	0.2	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 kΩ)	2000		V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (DC)		2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 2.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-220FP	DPAK IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.78	5	1.78	°C/W
R_{thj-a}	Thermal resistance junction-ambient max	62.5		100	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ °C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	170	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	800			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = max rating, V _{DS} = max rating, T _c = 125 °C			1 50	μA μA
I _{GSS}	Gate body leakage current (V _{GS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 1.25 A		3.8	4.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15 V, I _D = 1.25 A	-	2.1	-	S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	485 57 11	-	pF pF pF
C _{oss eq.} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 640 V	-	22	-	pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Off-voltage rise time Fall time	V _{DD} = 400 V, I _D = 1.25 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 19)	-	17 27 36 40	-	ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 640 V, I _D = 2.5 A V _{GS} = 10 V	-	19 3.2 10.8	-	nC nC nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%
2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		2.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		10	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=2.5\text{ A}$, $V_{GS}=0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=2.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=50\text{ V}$ (see Figure 21)	-	384		ns
Q_{rr}	Reverse recovery charge			1600		μC
I_{RRM}	Reverse recovery current			8.4		A
t_{rr}	Reverse recovery time	$I_{SD}=2.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=50\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 21)	-	474		ns
Q_{rr}	Reverse recovery charge			2100		μC
I_{RRM}	Reverse recovery current			8.8		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs}=\pm 1\text{ mA}$ (open drain)	30	-	-	V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, DPAK, IPAK

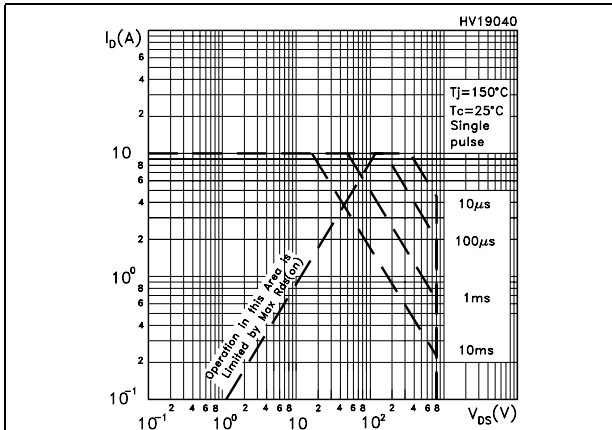


Figure 3. Thermal impedance for TO-220, DPAK, IPAK

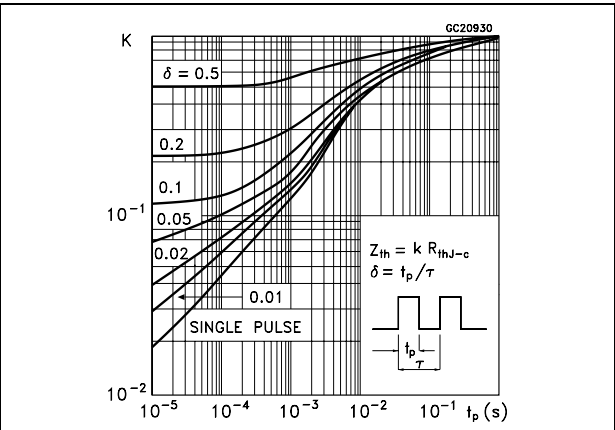


Figure 4. Safe operating area for TO-220FP

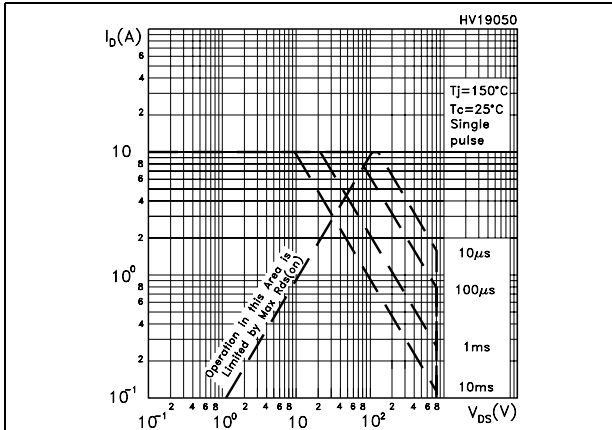


Figure 5. Thermal impedance for TO-220FP

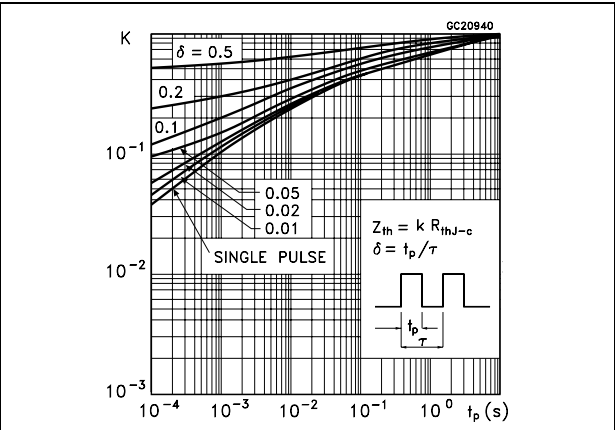


Figure 6. Output characteristics

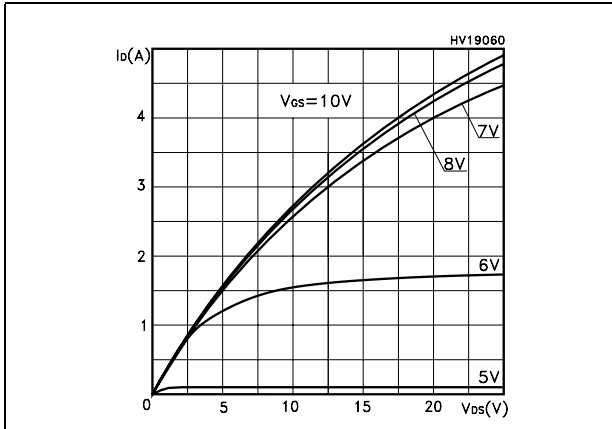


Figure 7. Transfer characteristics

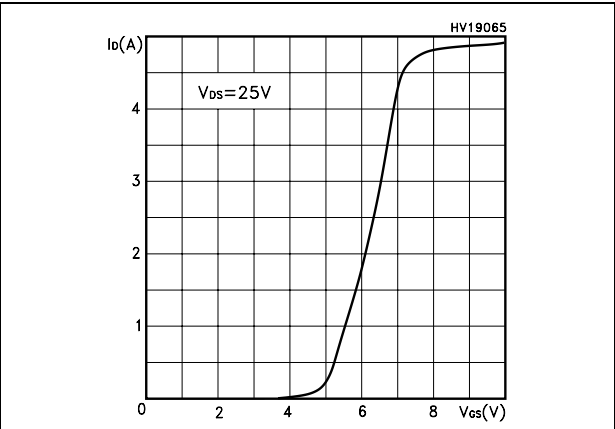


Figure 8. Transconductance

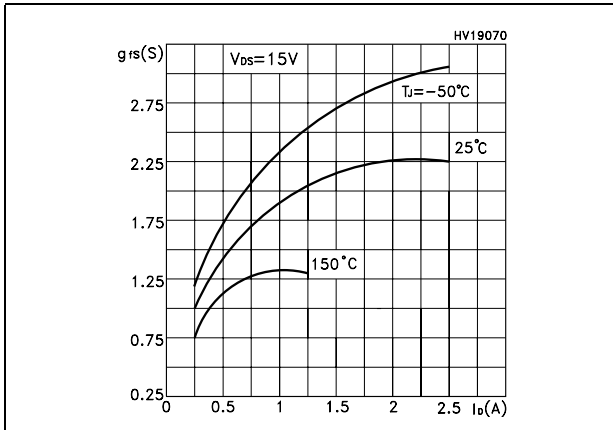


Figure 9. Static drain-source on resistance

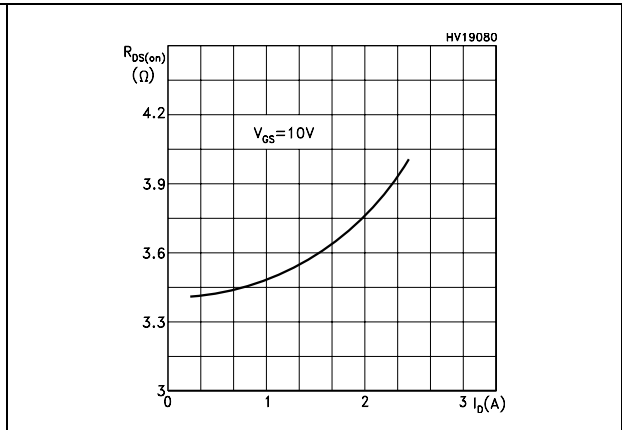


Figure 10. Gate charge vs gate-source voltage Figure 11. Capacitance variations

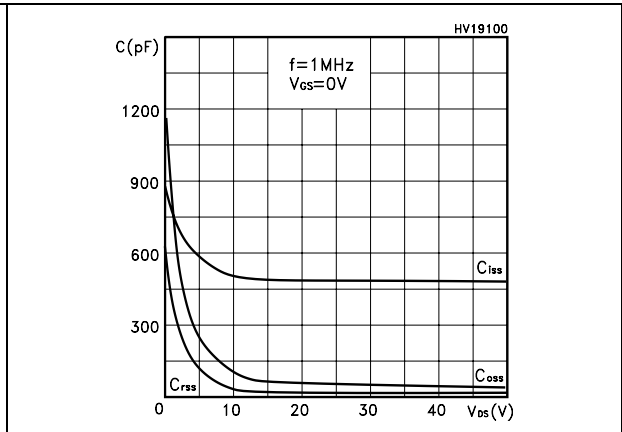
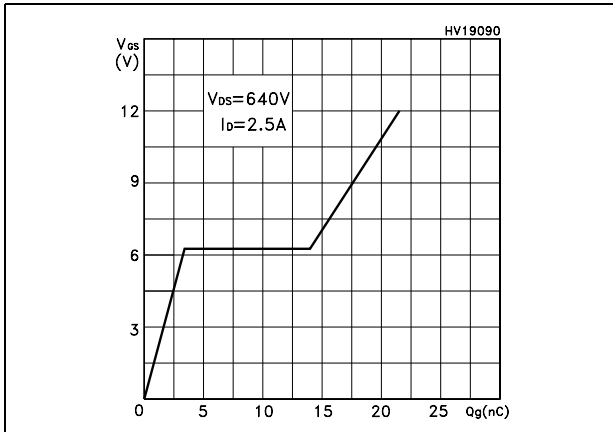


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized on resistance vs temperature

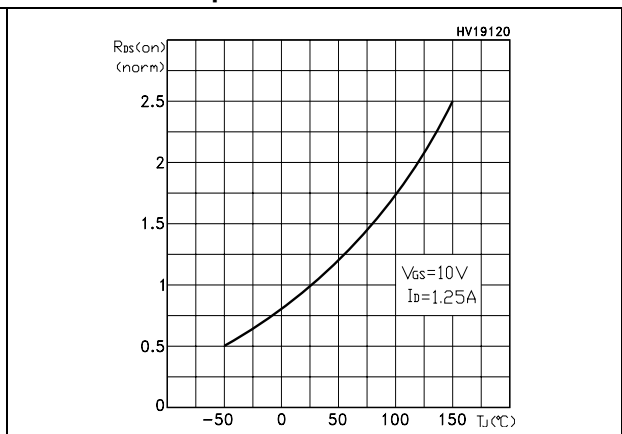
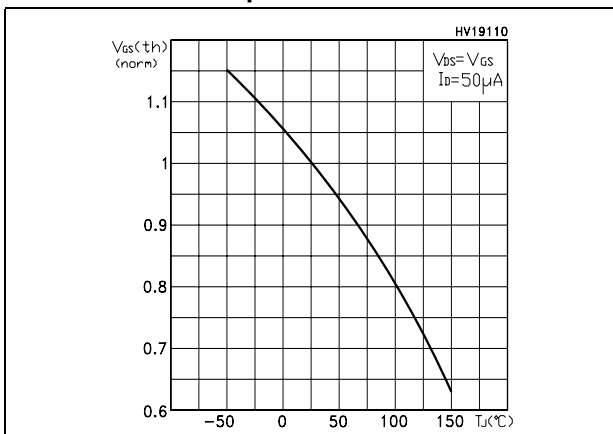


Figure 14. Source-drain diode forward characteristics

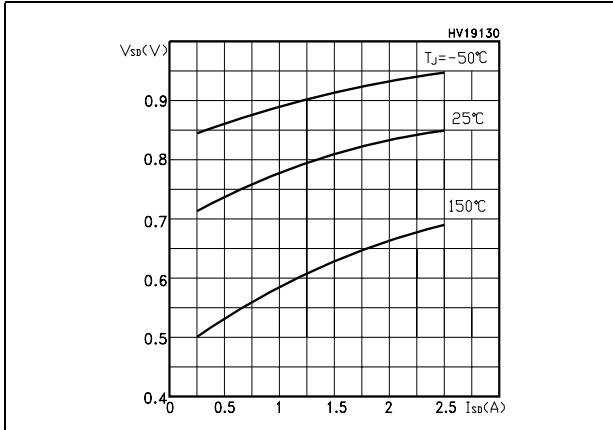


Figure 15. Normalized B_VDSS vs temperature

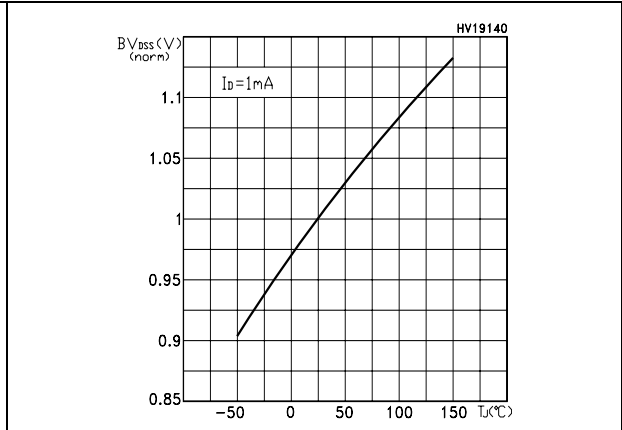
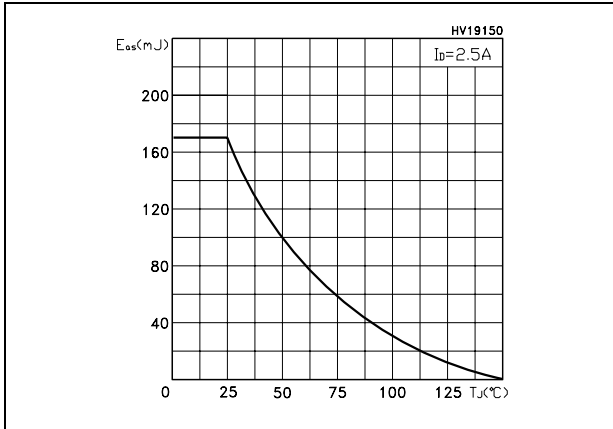


Figure 16. Maximum avalanche energy vs temperature



3 Test circuits

Figure 17. Switching times test circuit for resistive load

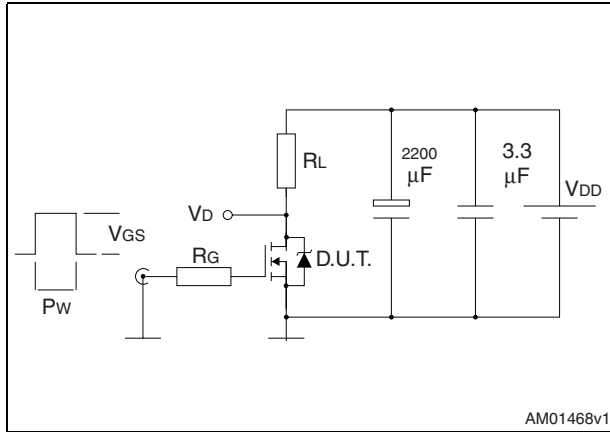


Figure 18. Gate charge test circuit

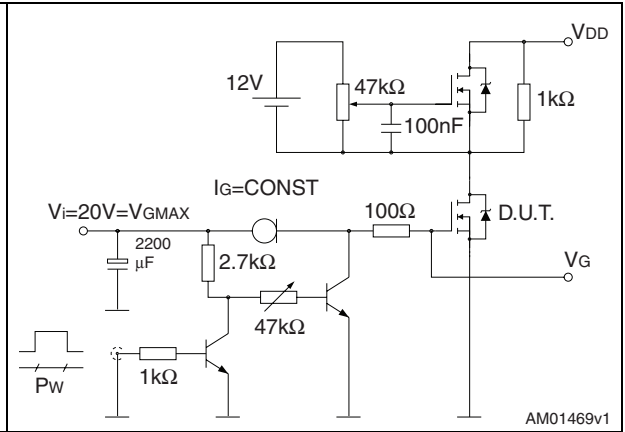


Figure 19. Test circuit for inductive load switching and diode recovery times

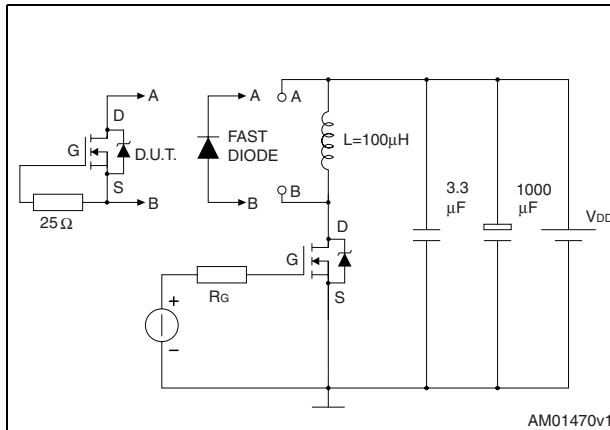


Figure 20. Unclamped inductive load test circuit

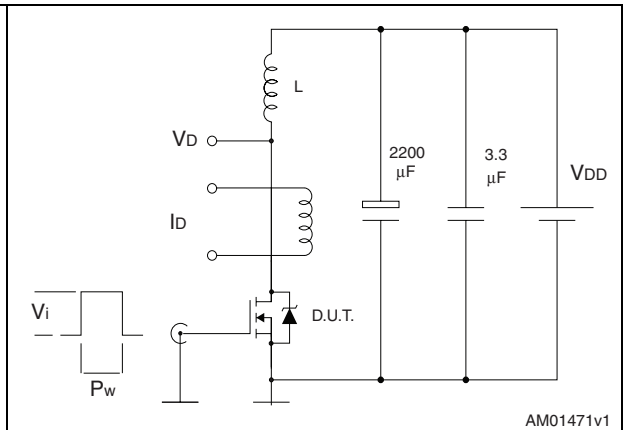


Figure 21. Unclamped inductive waveform

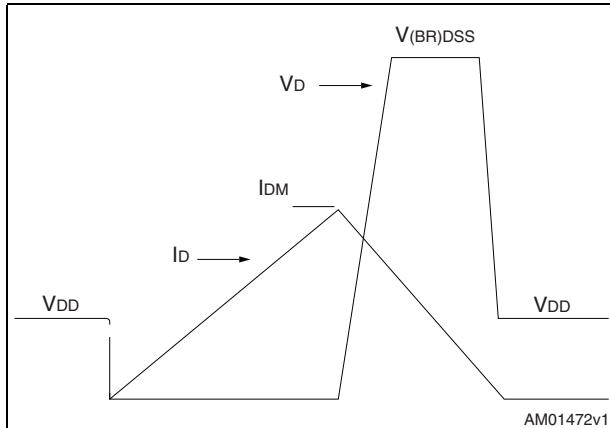
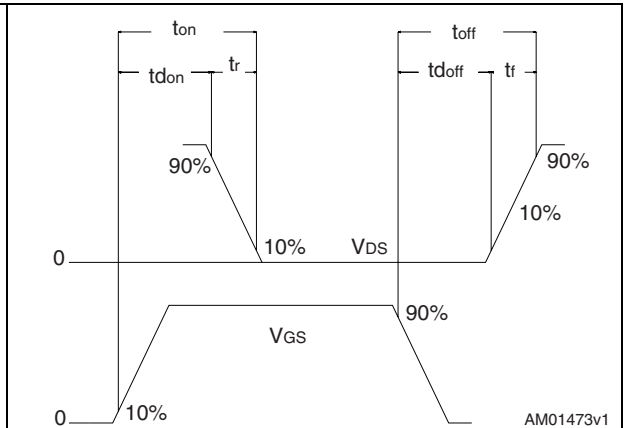


Figure 22. Switching time waveform

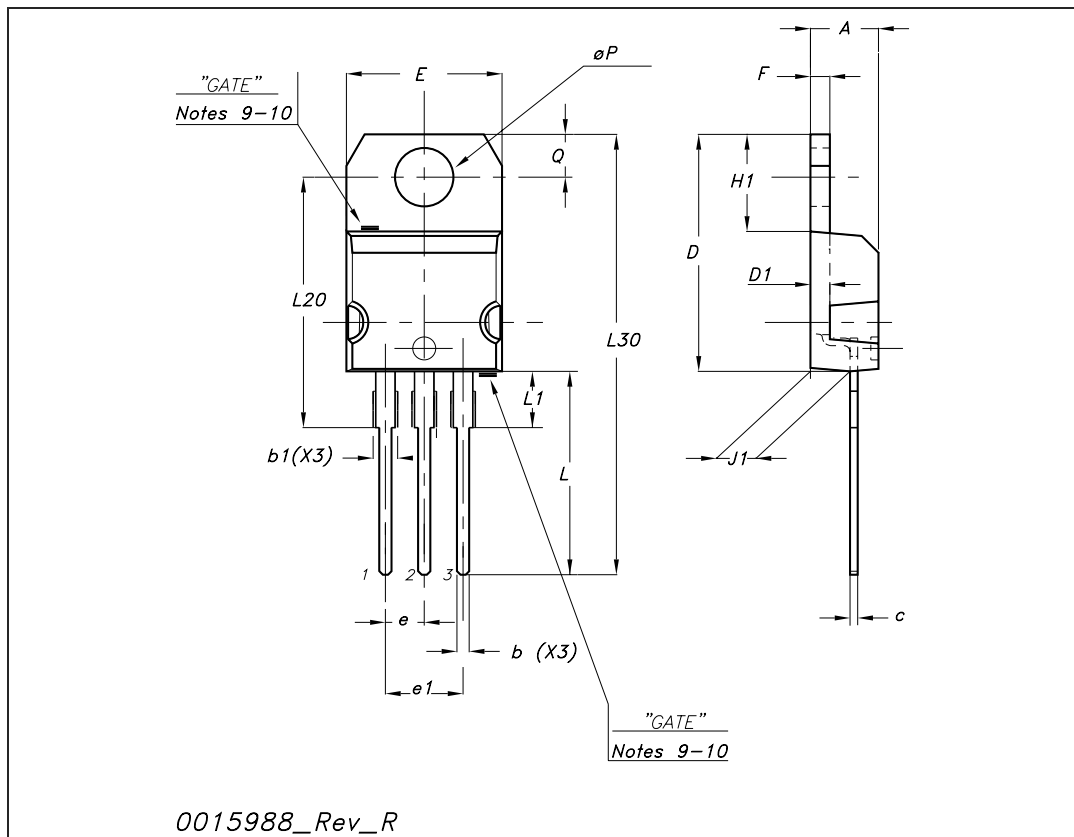


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

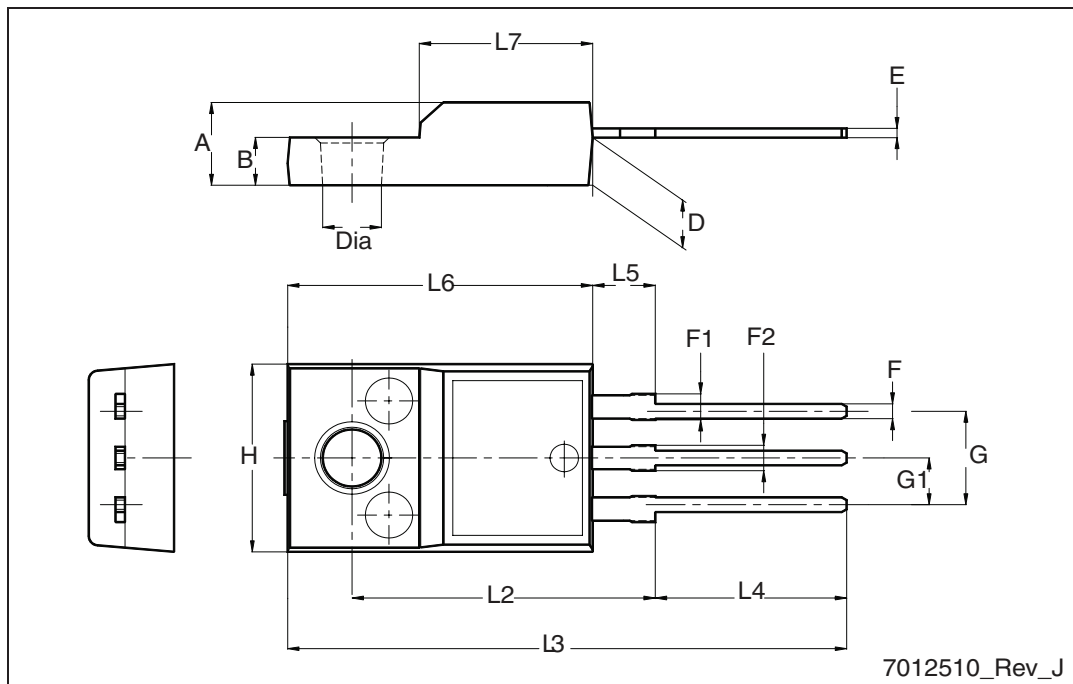
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



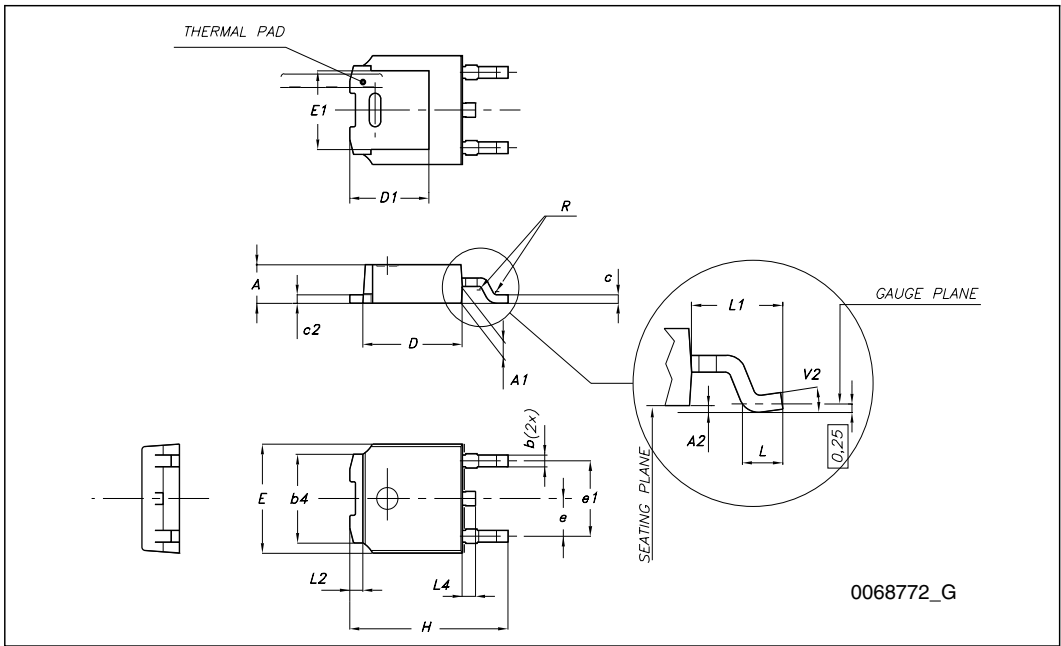
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



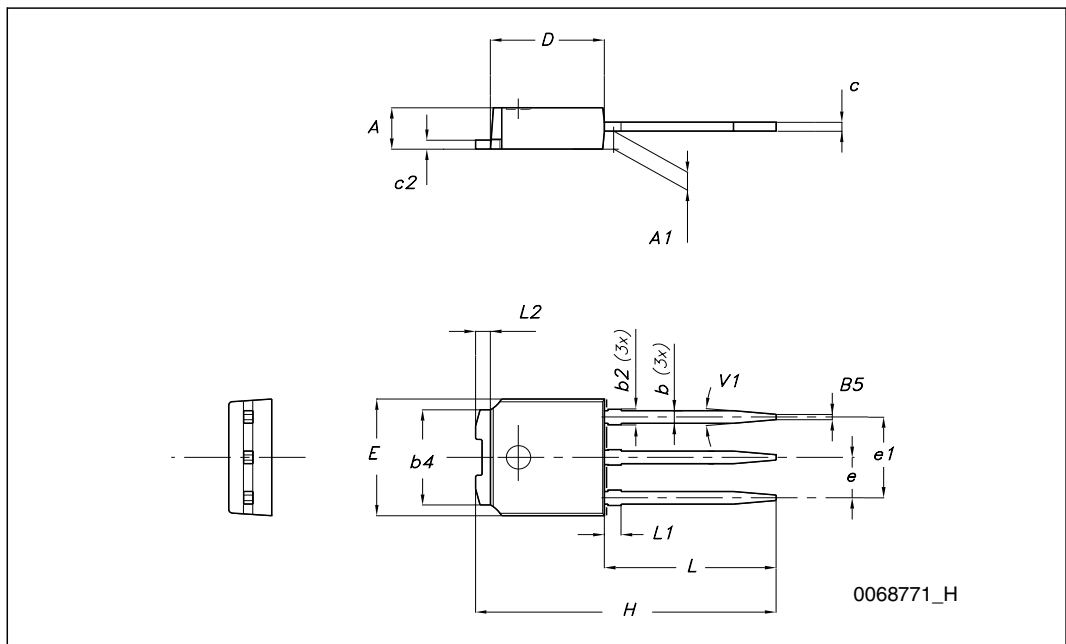
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



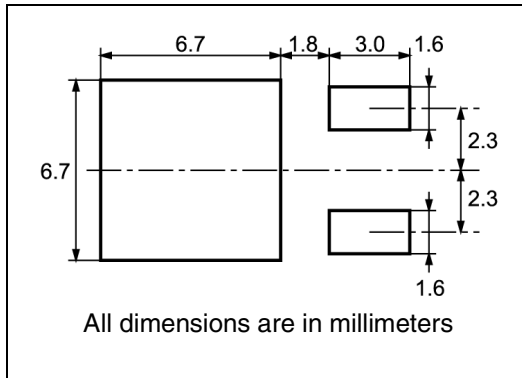
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

6 Revision history

Table 9. Revision history

Date	Revision	Changes
09-Sep-2004	3	Complete document
10-Aug-2006	4	New template, no content change
26-Feb-2009	5	Updated mechanical data
07-Sep-2009	6	$V_{ESD(G-S)}$ value has been corrected

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