

2SK408, 2SK409

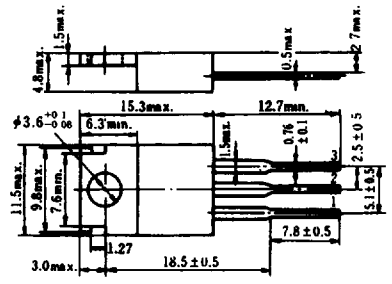
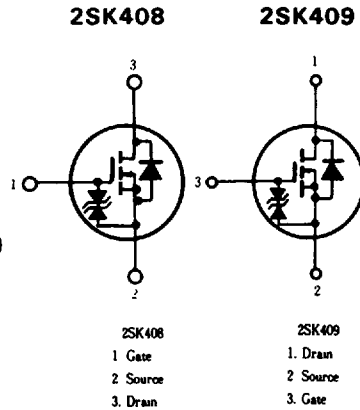
SILICON N-CHANNEL MOS FET

HITACHI/LOPTOELECTRONIC

HF/VHF POWER AMPLIFIER

■ **FEATURES**

- High Breakdown Voltage.
- You Can Decrease Handling Current.
- Included Gate Protection Diode.
- No Secondary-Breakdown.
- Wide A.S.O. (Area of Safe Operation)
- Simple Bias Circuitry
- No Thermal Runaway.



(Dimensions in mm)

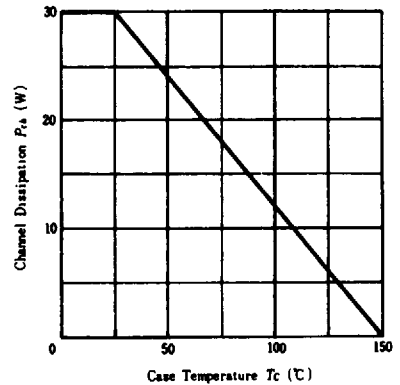
(JEDEC TO-220AB)

■ **ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$)**

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	180	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current	I_D	2	A
Channel Dissipation	P_{ch}^*	30	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \sim +150$	$^\circ\text{C}$

*Value at $T_c=25^\circ\text{C}$

POWER VS. TEMPERATURE DERATING

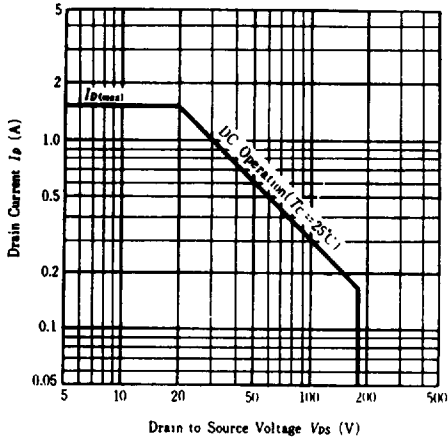


■ **ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$)**

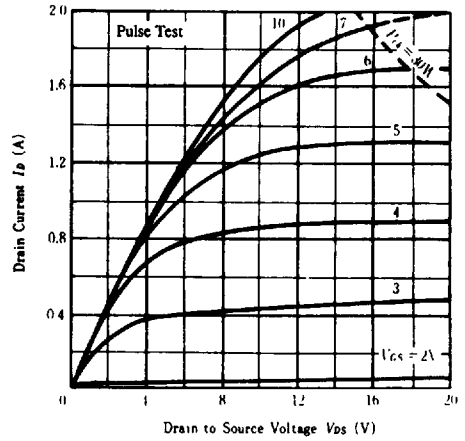
Item	Symbol	Test Condition	min.	typ.	max.	Unit
Power Output	P_O	$V_{DD}=80\text{V}, f=28\text{MHz}$	10	16	—	W
Drain Efficiency	η	$I_{DQ}=50\text{mA}, P_w=150\text{mW}$	—	80	—	%
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=10\text{mA}, V_{GS}=0$	180	—	—	V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$I_D=1\text{mA}, V_{DS}=10\text{V}$	0.5	—	3.0	V
Drain Current	I_{DSS}	$V_{DS}=140\text{V}, V_{GS}=0$	—	—	1.0	mA
Drain-Source Saturation Voltage	$V_{DS(on)}$	$I_D=1.0\text{A}, V_{GS}=10\text{V}^*$	—	6.5	8.0	V
Forward Transfer Admittance	$ y_f $	$I_D=1.0\text{A}, V_{DS}=20\text{V}^*$	0.2	0.3	—	S
Input Capacitance	C_{in}	$V_{GS}=5\text{V}, V_{DS}=0, f=1\text{MHz}$	—	100	—	pF
Output Capacitance	C_{out}	$V_{GS}=-5\text{V}, V_{DS}=50\text{V}, f=1\text{MHz}$	—	20	—	pF
Reverse Transfer Capacitance	C_{rs}	$V_{GD}=-50\text{V}, f=1\text{MHz}$	—	0.2	—	pF
Power Output	P_O	$V_{DD}=80\text{V}, f=28\text{MHz}$	—	10	—	W_{PEP}
Power Gain	P.G	$\Delta f=20\text{kHz}, \text{IMD} \leq -30\text{dB}$	—	20	—	dB

*Pulse Test

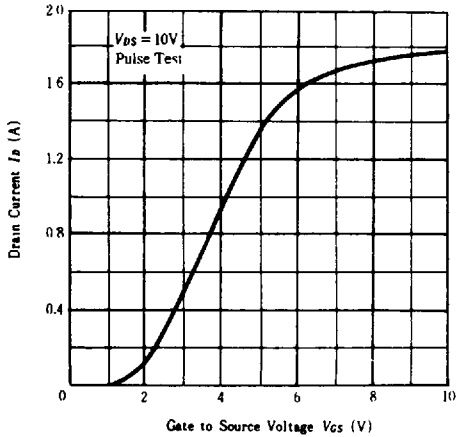
MAXIMUM SAFE OPERATION AREA



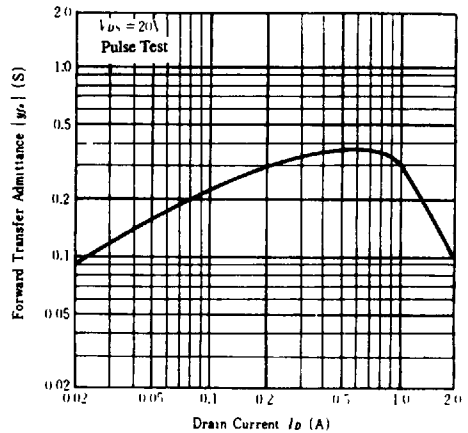
TYPICAL OUTPUT CHARACTERISTICS



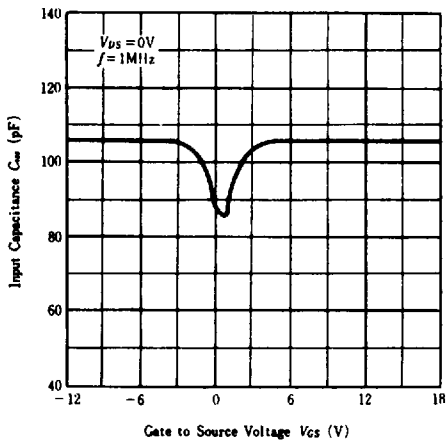
TYPICAL TRANSFER CHARACTERISTICS



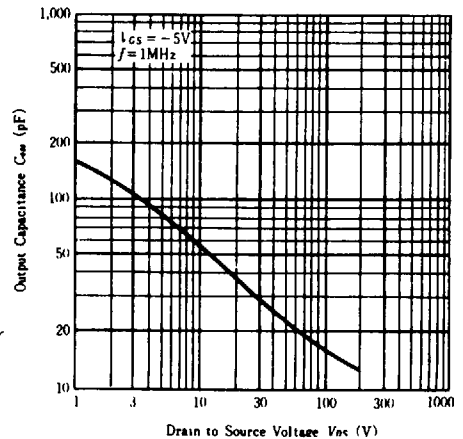
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



INPUT CAPACITANCE VS. GATE-SOURCE VOLTAGE

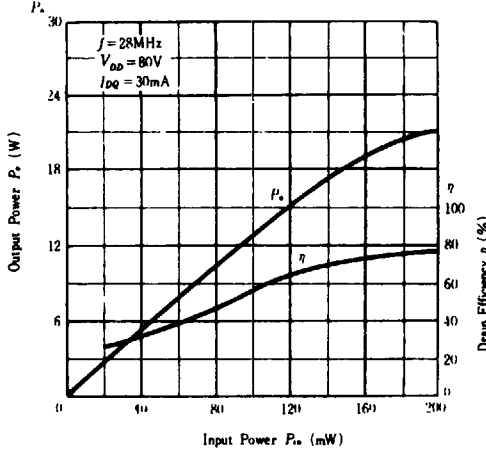


OUTPUT CAPACITANCE VS. DRAIN-SOURCE VOLTAGE

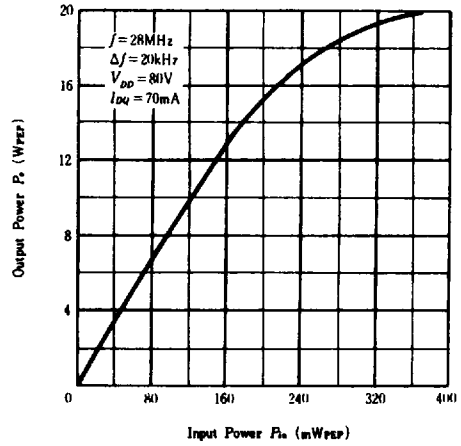


HITACHI/OPTOELECTRONIC BLE D

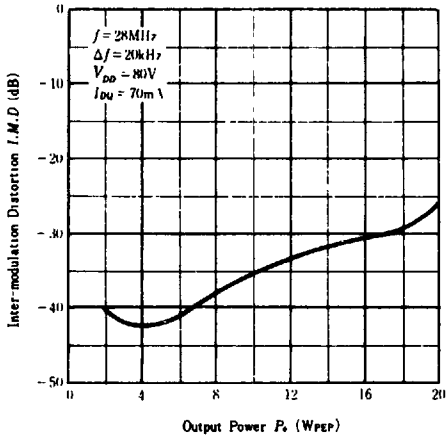
OUTPUT POWER, DRAIN EFFICIENCY VS. INPUT POWER



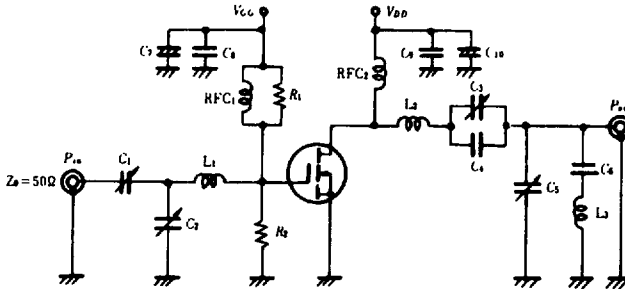
OUTPUT POWER VS. INPUT POWER (2 TONES)



INTER-MODULATION DISTORTION VS. OUTPUT POWER



28MHz Pout TEST CIRCUIT



- $C_1, C_2, C_3 \sim 50\text{pF}$
- $C_4 = 68\text{pF}$
- $C_5 = 20\text{pF}$
- $C_6 = 1.5\text{pF}$
- $C_7, C_8 = 0.1\mu\text{F}$
- $C_9 = 4.7\mu\text{F}$
- $C_{10} = 22\mu\text{F}$
- $L_1: ID=12\text{mm}, d=1.5\text{mm}, T=6T$
- $L_2: ID=12\text{mm}, d=1.5\text{mm}, T=9T$
- $L_3: ID=12\text{mm}, d=1.5\text{mm}, T=5T$